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 Krivokapic, Z.; Heavlin, W.D.;
 Semiconductor Manufacturing, IEEE Transactions on
 Volume 15, Issue 2, May 2002 Page(s):144 - 150
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- ☐ **2. Intra-field effects on device and circuit manufacturability: a statistical simulation**
 Krivokapic, Z.; Heavlin, W.D.;
 Semiconductor Manufacturing, IEEE Transactions on
 Volume 12, Issue 4, Nov. 1999 Page(s):437 - 451
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(280 KB\)](#) IEEE JNL
- ☐ **3. First silicon experiments within wafers**
 Heavlin, W.D.;
 Semiconductor Manufacturing Conference Proceedings, 1999 IEEE International Symp
 11-13 Oct. 1999 Page(s):375 - 378
[AbstractPlus](#) | Full Text: [PDF\(164 KB\)](#) IEEE CNF
- ☐ **4. Intrafield effects and device manufacturability: a statistical simulation approach**
 Krivokapic, Z.; Minvielle, A.; Heavlin, W.D.;
 Statistical Metrology, 1998. 3rd International Workshop on
 7 June 1998 Page(s):36 - 39
[AbstractPlus](#) | Full Text: [PDF\(204 KB\)](#) IEEE CNF


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Display Format: ☒ Citation ☐ Citation & Abstract

IEEE CNF IEEE Conference Proceeding

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**1. Statistically based parametric yield prediction for integrated circuits**

Gibson, D.S.; Poddar, R.; May, G.S.; Brooke, M.A.; Semiconductor Manufacturing, IEEE Transactions on Volume 10, Issue 4, Nov. 1997 Page(s):445 - 458

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(320 KB\)](#) IEEE JNL

IEEE STD IEEE Standard

**2. A methodology for the simultaneous design of supply and signal networks**

Haihua Su; Jiang Hu; Sapatnekar, S.S.; Nassif, S.R.; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 23, Issue 12, Dec. 2004 Page(s):1614 - 1624

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(776 KB\)](#) IEEE JNL**3. Redundancy modelling and array yield analysis for repairable embedded memori**

Sehgal, A.; Dubey, A.; Marinissen, E.J.; Wouters, C.; Vranken, H.; Chakrabarty, K.; Computers and Digital Techniques, IEE Proceedings-Volume 152, Issue 1, 14 Jan. 2005 Page(s):97 - 106

[AbstractPlus](#) | Full Text: [PDF\(1104 KB\)](#) IEEE JNL**4. Yield analysis for repairable embedded memories**

Sehgal, A.; Dubey, A.; Marinissen, E.J.; Wouters, C.; Vranken, H.; Chakrabarty, K.; European Test Workshop, 2003. Proceedings. The Eighth IEEE 25-28 May 2003 Page(s):35 - 40

[AbstractPlus](#) | Full Text: [PDF\(345 KB\)](#) IEEE CNF**5. Study of FSG/SiO/sub 2/ double interlayer conditions to prevent Al wiring delami 0.18-/spl mu/m device integration**

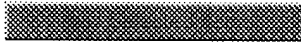
Kawashima, Y.; Ichikawa, T.; Nakamura, N.; Obata, S.; Den, Y.; Kawano, H.; Ide, T.; K Semiconductor Manufacturing, IEEE Transactions on Volume 15, Issue 4, Nov. 2002 Page(s):497 - 505

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(867 KB\)](#) IEEE JNL**6. EM-based optimization of microwave circuits using artificial neural networks: the Rayas-Sanchez, J.E.;**

Microwave Theory and Techniques, IEEE Transactions on Volume 52, Issue 1, Jan. 2004 Page(s):420 - 435

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(1184 KB\)](#) IEEE JNL

- ☐ 7. **Crosstalk and microlens study in a color CMOS image sensor**
Agranov, G.; Berezin, V.; Tsai, R.H.;
Electron Devices, IEEE Transactions on
Volume 50, Issue 1, Jan. 2003 Page(s):4 - 11
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(1666 KB\)](#) IEEE JNL
- ☐ 8. **Parametric manufacturing yield modeling of GaAs/AlGaAs multiple quantum well photodiodes**
Ilgu Yun; May, G.S.;
Semiconductor Manufacturing, IEEE Transactions on
Volume 12, Issue 2, May 1999 Page(s):238 - 251
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(432 KB\)](#) IEEE JNL
- ☐ 9. **Thin film transistors for foldable displays**
Ma, E.Y.; Theiss, S.D.; Lu, M.H.; Wu, C.C.; Sturn, J.C.; Wagner, S.;
Electron Devices Meeting, 1997. Technical Digest., International
7-10 Dec. 1997 Page(s):535 - 538
[AbstractPlus](#) | Full Text: [PDF\(260 KB\)](#) IEEE CNF
- ☐ 10. **DGPS/INS integrated positioning for control of automated vehicle**
Redmill, K.A.; Kitajima, T.; Ozguner, U.;
Intelligent Transportation Systems, 2001. Proceedings. 2001 IEEE
25-29 Aug. 2001 Page(s):172 - 178
[AbstractPlus](#) | Full Text: [PDF\(592 KB\)](#) IEEE CNF



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6239912, B1999-06-2570-009; 19990501.

Title

Enhancing fab performance under team council methodology.

Author(s)[Dupuis-R-N-Jr](#); [Gervais-J](#); [Park-S](#).**Author affiliation**

Fairchild Semicond, South Portland, ME, USA.

SourceIEEE/SEMI. 1998 IEEE/SEMI Advanced **Semiconductor Manufacturing** Conference and Workshop, Boston, MA, USA, 23-25 Sept. 1998.

Sponsors: Semicond. Equipment & Mater. Int. (SEMI), IEEE, IEEE Electron Devices Soc., IEEE Components, Packaging & Manuf. Technol. Soc.

In: p.119-21, 1998.

ISSN

ISBN: 0-7803-4380-8, CCCC: 0 7803 4380 8/98/ (\$10.00).

Publication year

1998.

Language

EN.

Publication type

CPP Conference Paper.

Treatment codes

P Practical.

Abstract

The objective of this paper is to outline and describe the process of developing team councils in a wafer fab organization. Initially, we present the historical background and why we thought this type of approach was necessary to achieve high performance from all levels of the organization. A road **map** to success as well as a task level migration **matrix** describes the different levels of responsibility needed to achieve the results described in the conclusion of this paper. Though this process is still evolving and developing in the authors' South Portland fab, the paper describes the necessary steps to implement this process. (3 refs).

Descriptors

[computer-integrated-manufacturing](#); [integrated-circuit-reliability](#);
[integrated-circuit-technology](#); [integrated-circuit-yield](#); [management](#);
[manufacturing-resources-planning](#); [training](#).

Keywords

wafer fab performance; team council methodology; wafer fab organization; team councils; road map; task level migration **matrix**; responsibility levels; process implementation; training; CIM.

Classification codes

B2570 (Semiconductor integrated circuits).
B0170E (Production facilities and engineering).
B0170N (Reliability).
B0140 (Administration and management).
B0120 (Education and training).

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4275011, C9212-7480-045; 921104.

Title

Semi-conductor integrated technical data manager.

Author(s)[Gagliardi-D-J](#); [Kleinman-Y-N](#).**Author affiliation**

IBM, Hopewell Jct, NY, USA.

SourceEleventh IEEE/CHMT International Electronics **Manufacturing** Technology Symposium (Cat. No.91CH3043-7), San Francisco, CA, USA, 16-18 Sept. 1991, p.222-5.

Sponsors: IEEE.

Published: IEEE, New York, NY, USA, 1991, xvi+449 pp.

ISSN

ISBN: 0-7803-0155-2, CCCC: CH3043-7/91/0000-0222 (\$01.00).

Publication year

1991.

Language

EN.

Publication type

CPP Conference Paper.

Treatment codes

P Practical.

Abstract

The author describes the architecture of the Semi-Conductor Integrated Technical Data Manager (SCIM) system. SCIM is a design automation system that integrates data and controls the processes that are required for the release of the masterslice to **manufacturing**. The two key components of the system are the relational database and its functional controller. As the data are generated by the design community, the relational database allows for the integration of all independent data elements across the design life cycle. The functional controller ensures the integrity of the process and that it is in compliance with the ground-rule specifications. In particular, the authors address the creation and integration of the product **matrix**, the wafer **map** (or stepping plan), and the technology ground rules, which are all central to the release of masterslice design data to **manufacturing**. (3 refs).

Descriptors[CAD-CAM](#); [integrated-circuit-manufacture](#); [process-computer-control](#);
[relational-databases](#); [semiconductor-device-manufacture](#).

Keywords

Semi Conductor Integrated Technical Data Manager; SCIM; design automation system; masterslice; relational database; functional controller; product **matrix**; wafer **map**; stepping plan; technology ground rules.

Classification codes

C7480 (Production engineering).
C3355Z (Other **manufacturing** processes).
C7420 (Control engineering).
C7410D (Electronic engineering).
C6160D (Relational DBMS).

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2001. (INZZ) Layout manufacturability analysis using rigorous 3-d topography simulation.

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1987. (INZZ) On stabilizing the final test programs of integrated circuits.

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7820829, B2004-02-2560-002; 20040101.

Title

Designing experiments for causal networks.

Author(s)[Heavlin-W-D.](#)**Author affiliation**

Adv Micro Devices, Granada, Spain.

Source

Technometrics (USA), vol.45, no.2, p.115-29, May 2003. , Published: American Soc. Quality Control; American Stat. Assoc.

CODEN

TCMTA2.

ISSN

ISSN: 0040-1706.

Availability

SICI: 0040-1706(200305)45:2L:115:DECN; 1-F.

Publication year

2003.

Language

EN.

Publication type

J Journal Paper.

Treatment codes

A Application.

Abstract

Causal networks are directed graphs representing cause-effect relationships and are multiple-response generalizations of Ishikawa's cause-effect diagrams. Emphasizing tolerance design applications, this article describes an algorithm for designing suitable experiments when the factors and responses are organized as a causal network. The causal network is transformed into a so-called causal map, which represents all factors and responses as points in a common D-dimensional metric space. The design approach is algorithmic, optimizing the entropy criterion due to Wynn. This criterion is applied to maximize dispersion among the multiple responses, using a distance-in-space coefficients model. A key constraint is for the blocks to be self-contained; this implies that each block can be analyzed without

reference to other blocks. This is to be complemented by a unified, all-block analysis. The resulting designs are evaluated for efficiency, response dispersion, and resolution V column rank. Particular attention is given to skewing each block by shifting one or a few factors off-center. (22 refs).

Descriptors

causality; cause-effect-analysis; process-control; semiconductor-device-manufacture.

Keywords

causal networks; directed graphs; cause effect relationships; multiple response generalizations; Ishikawa s cause effect diagrams; tolerance design applications; common D dimensional metric space; multiple responses; distance in space coefficients model; efficiency; response dispersion.

Classification codes

B2560 (Semiconductor devices).

B0170E (Production facilities and engineering).

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File: PGPB

Jan 16, 2003

PGPUB-DOCUMENT-NUMBER: 20030014144

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030014144 A1

TITLE: FEED-FORWARD CONTROL OF TCI DOPING FOR IMPROVING MASS-PRODUCTION-WISE,
STATISTICAL DISTRIBUTION OF CRITICAL PERFORMANCE PARAMETERS IN SEMICONDUCTOR
DEVICES

PUBLICATION-DATE: January 16, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Krivokapic, Zoran	Santa Clara	CA	US	
Heavlin, William D.	El Granada	CA	US	

US-CL-CURRENT: 700/121; 700/44

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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L1: Entry 2 of 12

File: USPT

Mar 16, 2004

US-PAT-NO: 6708073

DOCUMENT-IDENTIFIER: US 6708073 B1

TITLE: Lot specific process design methodology

DATE-ISSUED: March 16, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Heavlin, William D.	El Granada	CA		

US-CL-CURRENT: 700/121; 700/31

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw De
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☐ 3. Document ID: US 6586755 B1

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File: USPT

Jul 1, 2003

US-PAT-NO: 6586755

DOCUMENT-IDENTIFIER: US 6586755 B1

TITLE: Feed-forward control of TCI doping for improving mass-production-wise statistical distribution of critical performance parameters in semiconductor devices

DATE-ISSUED: July 1, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Krivokapic; Zoran	Santa Clara	CA		
Heavlin; William D.	El Granada	CA		

US-CL-CURRENT: 250/492.21; 250/492.23, 257/E21.525, 438/5, 438/7

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D
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☒ 4. Document ID: US 6567717 B2

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File: USPT

May 20, 2003

US-PAT-NO: 6567717

DOCUMENT-IDENTIFIER: US 6567717 B2

TITLE: Feed-forward control of TCI doping for improving mass-production-wise, statistical distribution of critical performance parameters in semiconductor devices

DATE-ISSUED: May 20, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Krivokapic; Zoran	Santa Clara	CA		
Heavlin; William D.	El Granada	CA		

US-CL-CURRENT: 700/121; 438/14

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D
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☒ 5. Document ID: US 6389366 B1

L1: Entry 5 of 12

File: USPT

May 14, 2002

US-PAT-NO: 6389366

DOCUMENT-IDENTIFIER: US 6389366 B1

TITLE: Methods for identifying sources of patterns in processing effects in manufacturing

DATE-ISSUED: May 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Heavlin; William D.	El Granada	CA		

US-CL-CURRENT: 702/84; 438/21, 700/117, 702/81

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWAC	Draw De
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☐ 6. Document ID: US 6366822 B1

L1: Entry 6 of 12

File: USPT

Apr 2, 2002

US-PAT-NO: 6366822

DOCUMENT-IDENTIFIER: US 6366822 B1

TITLE: Statistical process window design methodology

DATE-ISSUED: April 2, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Heavlin; William D.	El Granada	CA		

US-CL-CURRENT: 700/31; 700/121

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWAC	Draw De
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☒ 7. Document ID: US 6304836 B1

L1: Entry 7 of 12

File: USPT

Oct 16, 2001

US-PAT-NO: 6304836

DOCUMENT-IDENTIFIER: US 6304836 B1

**** See image for Certificate of Correction ****

TITLE: Worst case design parameter extraction for logic technologies

DATE-ISSUED: October 16, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Krivokapic; Zoran	Santa Clara	CA		
Heavlin; William D.	El Granada	CA		

US-CL-CURRENT: 703/14; 703/13

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D.
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☒ 8. Document ID: US 5966527 A

L1: Entry 8 of 12

File: USPT

Oct 12, 1999

US-PAT-NO: 5966527

DOCUMENT-IDENTIFIER: US 5966527 A

TITLE: Apparatus, article of manufacture, method and system for simulating a mass-produced semiconductor device behavior

DATE-ISSUED: October 12, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Krivokapic; Zoran	Santa Clara	CA		
Heavlin; William D.	San Francisco	CA		

US-CL-CURRENT: 703/14

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D.
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☐ 9. Document ID: US 5946214 A

L1: Entry 9 of 12

File: USPT

Aug 31, 1999

US-PAT-NO: 5946214

DOCUMENT-IDENTIFIER: US 5946214 A

TITLE: Computer implemented method for estimating fabrication yield for semiconductor integrated circuit including memory blocks with redundant rows and/or columns

DATE-ISSUED: August 31, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Heavlin; William D.	San Francisco	CA		
Kittler; Richard C.	Sunnyaale	CA		
Wen; Ping	Sunnyvale	CA		

US-CL-CURRENT: 700/121; 365/200, 365/201, 700/95, 700/96

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D.
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☒ 10. Document ID: US 5724251 A

L1: Entry 10 of 12

File: USPT

Mar 3, 1998

US-PAT-NO: 5724251

DOCUMENT-IDENTIFIER: US 5724251 A

TITLE: System and method for designing, fabricating and testing multiple cell test structures to validate a cell library

DATE-ISSUED: March 3, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
<u>Heavlin</u> ; William D.	San Francisco	CA		

US-CL-CURRENT: 716/5; 716/11

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw De
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☒ 11. Document ID: US 5655110 A

L1: Entry 11 of 12

File: USPT

Aug 5, 1997

US-PAT-NO: 5655110

DOCUMENT-IDENTIFIER: US 5655110 A

**** See image for Certificate of Correction ****

TITLE: Method for setting and adjusting process parameters to maintain acceptable critical dimensions across each die of mass-produced semiconductor wafers

DATE-ISSUED: August 5, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Krivokapic; Zoran	Santa Clara	CA		
<u>Heavlin</u> ; William D.	San Francisco	CA		
Kyser; David F.	San Jose	CA		

US-CL-CURRENT: 716/19; 700/95, 703/13

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw De
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☒ 12. Document ID: US 5646870 A

L1: Entry 12 of 12

File: USPT

Jul 8, 1997

US-PAT-NO: 5646870

DOCUMENT-IDENTIFIER: US 5646870 A

**** See image for Certificate of Correction ****

TITLE: Method for setting and adjusting process parameters to maintain acceptable critical dimensions across each die of mass-produced semiconductor wafers

DATE-ISSUED: July 8, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Krivokapic; Zoran	Santa Clara	CA		
Heavlin; William D.	San Francisco	CA		
Kyser; David F.	San Jose	CA		

US-CL-CURRENT: 716/4; 700/117, 700/31, 703/13, 716/20

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KM/C	Draw D
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☐ 1. Document ID: US 20040064438 A1

L2: Entry 1 of 2

File: PGPB

Apr 1, 2004

PGPUB-DOCUMENT-NUMBER: 20040064438

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040064438 A1

TITLE: Method for data and text mining and literature-based discovery

PUBLICATION-DATE: April 1, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kostoff, Ronald N.	Arlington	VA	US	

US-CL-CURRENT: 707/1

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 2. Document ID: US 6886010 B2

L2: Entry 2 of 2

File: USPT

Apr 26, 2005

US-PAT-NO: 6886010

DOCUMENT-IDENTIFIER: US 6886010 B2

TITLE: Method for data and text mining and literature-based discovery

DATE-ISSUED: April 26, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kostoff; Ronald N.	Arlington	VA		

US-CL-CURRENT: 707/3; 707/10, 707/4, 707/6

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw D
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